IN THE CLAIMS

Please **amend** Claims 1-2, 4, 6-8, 10, 12-14, 16 and 18 as indicated:

1. (currently amended) A method for testing an integrated circuit, the method comprising:

grouping a circuit logic into one or more logic areas;

associating each one of the logic areas with one or more first testcases;

altering a circuit in one of the logic areas to create an altered logic area from an unaltered said one or more logic [[area]] areas;

[[retesting]] testing the altered logic area using only [[with]] the one or more first testcases associated with the unaltered logic area;

identifying failed first testcases; and

counting the number of logic areas in the failed first testcases to predict which logic areas are adversely affected by the altering of the circuit.

2. (currently amended) The method of claim 1, further comprising:

identifying other logic area utilized by the [[filed]] failed first testcases, the other logic area being different from the altered logic area;

[[re-running]] running at least one second testcase that tests the other logic [[areas]] area;

identifying the second testcases that fail; and

identifying common logic areas affected by the failed second testcases and the failed first testcases to predict which logic areas are adversely affected by the altering of the circuit.

3. (original) The method of claim 2, wherein the failed first and second testcases are mapped on a scoreboard that affords a visual view of a relationship among affected logic areas to predict which logic areas are defective.

4. (currently amended) The method of claim [[1]] 2, wherein the predicting of which logic areas are adversely affected is achieved by identifying a common logic area in both the first and second failed testcases.

5. (original) The method of claim 1, wherein the integrated circuit is a virtual circuit created by a hardware descriptor language.

6. (currently amended) The method of claim 1, further comprising:

running a new testcase on [[the circuit]] one of the logic areas in the circuit logic;

if the new testcase fails, examining other failed first testcases in other logic areas in the circuit logic; and

identifying a common logic area [[in the failed]] that failed the new testcase and the [[failed]] first testcases to predict a defect in the common logic area in the circuit logic.

7. (currently amended) A system for testing an integrated circuit, the system comprising:

means for grouping a circuit logic into one or more logic areas;

means for associating each one of the logic areas with one or more first testcases;

means for altering a circuit in one of the logic areas to create an altered logic area from an unaltered said one or more logic [[area]] areas;

means for [[retesting]] testing the altered logic area using only [[with]] the one or more first testcases associated with the unaltered logic area;

means for identifying failed first testcases; and

means for counting the number of logic areas in the failed first testcases to predict which logic areas are adversely affected by the altering of the circuit.

8. (currently amended) The system of claim 7, further comprising:

means for identifying other logic area utilized by the [[filed]] failed first testcases, the other logic area being different from the altered logic area;

means for [[re-running]] running at least one second testcase that tests the other logic [[areas]] area;

means for identifying the second testcases that fail; and

means for identifying common logic areas affected by the failed second testcases and the failed first testcases to predict which logic areas are adversely affected by the altering of the circuit.

9. (original) The system of claim 8, wherein the failed first and second testcases are mapped on a scoreboard that affords a visual view of a relationship among affected logic areas to predict which logic areas are defective.

10. (currently amended) The system of claim [[7]] 8, wherein the predicting of which logic areas are adversely affected is achieved by identifying a common logic area in both the first and second failed testcases.

11. (original) The system of claim 7, wherein the integrated circuit is a virtual circuit created by a hardware descriptor language.

12. (currently amended) The system of claim 7, further comprising:

means for running a new testcase on [[the circuit]] one of the logic areas in the circuit logic;

means for, if the new testcase fails, examining other failed first testcases in other logic areas in the circuit logic; and

means for identifying a common logic area [[in the failed]] that failed the new testcase and the [[failed]] first testcases to predict a defect in the common logic area in the circuit logic.

13. (currently amended) A computer program product, residing on a computer usable medium and executable on a computer, for testing an integrated circuit, the computer program product comprising:

program code for grouping a circuit logic into one or more logic areas;

program code for associating each one of the logic areas with one or more first testcases;

program code for altering a circuit in one of the logic areas to create an altered logic area from an unaltered said one or more logic [[area]] areas;

program code for [[retesting]] testing the altered logic area using only [[with]] the one or more first testcases associated with the unaltered logic area;

program code for identifying failed first testcases; and

program code for counting the number of logic areas in the failed first testcases to predict which logic areas are adversely affected by the altering of the circuit.

14. (currently amended) The computer program product of claim 13, further comprising:

program code for identifying other logic area utilized by the [[filed]] failed first testcases, the other logic area being different from the altered logic area;

program code for [[re-running]] running at least one second testcase that tests the other logic [[areas]] area;

program code for identifying the second testcases that fail; and

program code for identifying common logic areas affected by the failed second testcases and the failed first testcases to predict which logic areas are adversely affected by the altering of the circuit.

15. (original) The computer program product of claim 14, wherein the failed first and second testcases are mapped on a scoreboard that affords a visual view of a relationship among affected logic areas to predict which logic areas are defective.

16. (currently amended) The computer program product of claim [[13]] 14, wherein the predicting of which logic areas are adversely affected is achieved by identifying a common logic area in both the first and second failed testcases.

17. (original) The computer program product of claim 13, wherein the integrated circuit is a virtual circuit created by a hardware descriptor language.

18. (currently amended) The computer program product of claim 13, further comprising:

program code for running a new testcase on [[the circuit]] one of the logic areas in the circuit logic;

program code for, if the new testcase fails, examining other failed first testcases in other logic areas in the circuit logic; and

program code for identifying a common logic area [[in the failed]] that failed the new testcase and the [[failed]] first testcases to predict a defect in the common logic area in the circuit logic.